Design Data Browser (DDB) A High-Performance Interactive Environment for Timing Triage

Authors/Contributors (IBM)

Kerim Kalafala

Rob Allen
Chris Cavitt
Deb Dean
Mitch DeHond
Nate Hieter
Ed Hughes
Doug Keller
Anurag Kompalli
Richard Taggart

Motivation and Key Challenges

- *Challenge #1:* **Design Hierarchy**
  - *Timing Analysis is divided among hundreds of individual runs across the physical design hierarchy.*
  - *How to put all the pieces back together in an intuitive interactive debug environment ?*

- *Challenge #2:* **Visualization of both design and timing data**
  - *How does one efficiently visualize the design data including circuit placement and sizing, as well wiring, in a fashion that will naturally assist timing debug ?*

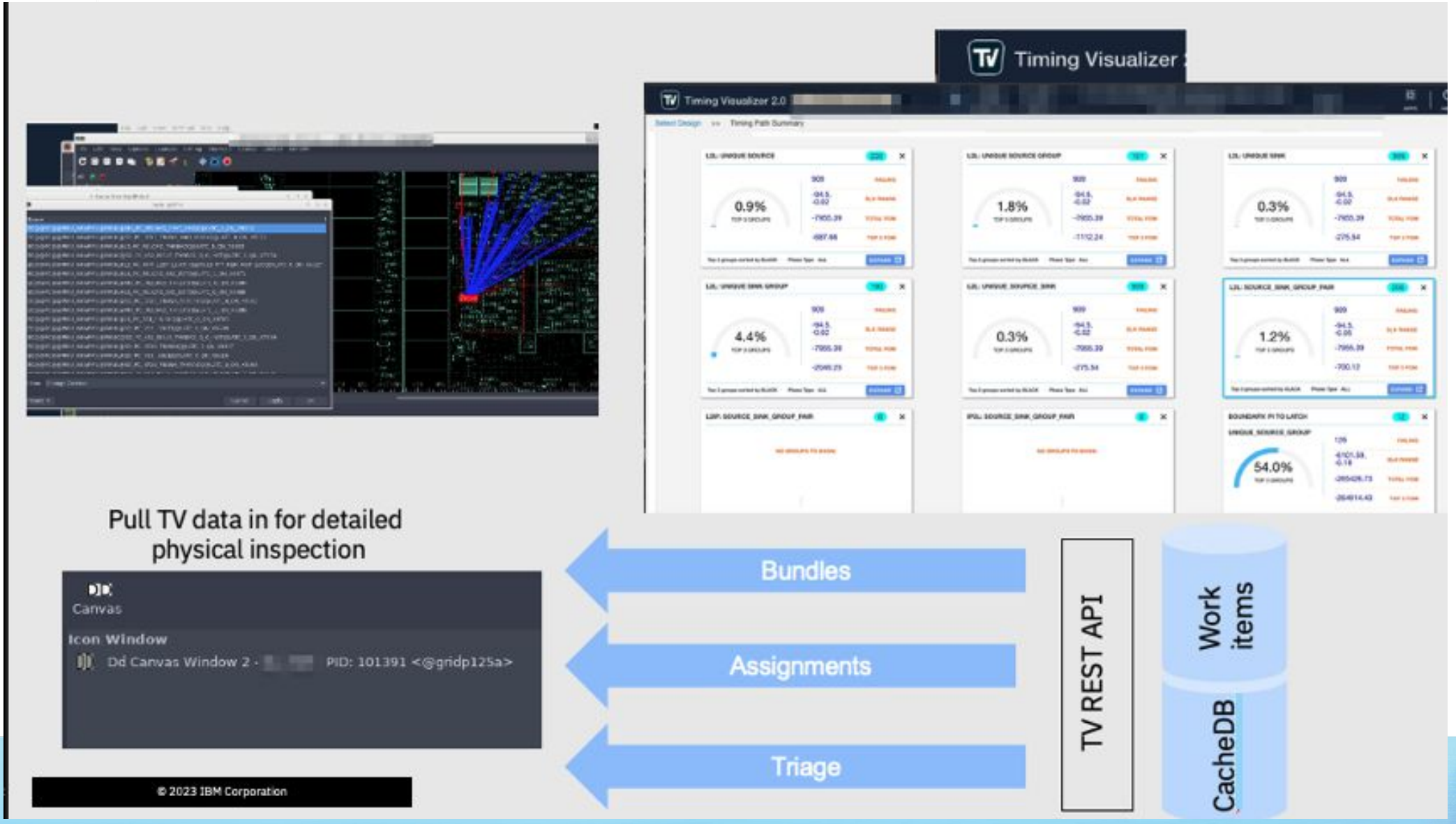
Motivation and Key Challenges

- *Challenge #3:* **Optimizing latch placement**
  - *What are the critical fan-in/out paths to/from a given latch ?*
  - *Should a latch be placed differently in order to improve timing ?*

- *Challenge #4:* **Multi-cycle path analysis**
  - *How to best optimize timing for across multiple latch-to-latch cycles ?*

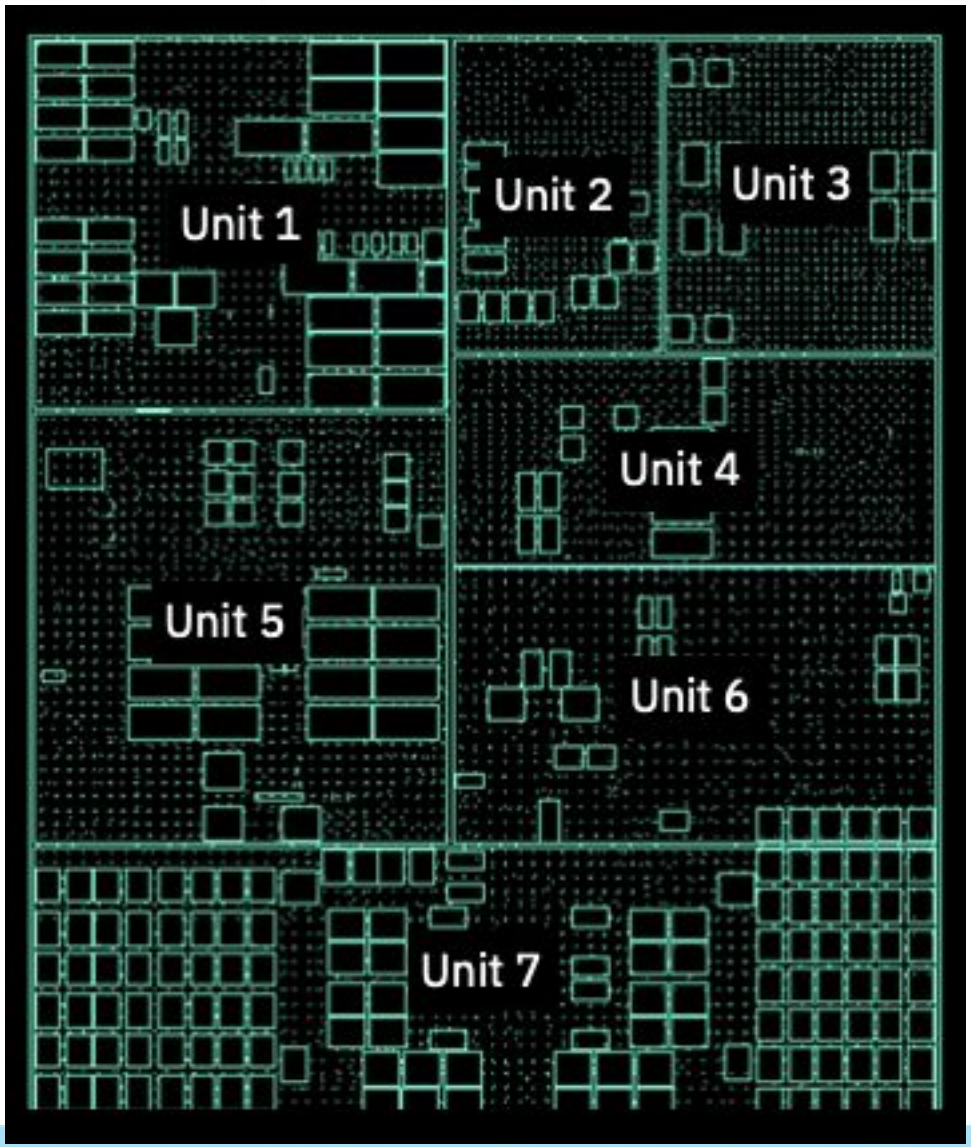
Key Innovation

Integrate existing web-based timing visualizer with a new X-windows based ***high-performance front end*** *for* ***exploring physical and timing data***



Hierarchical Integration of Timing and P

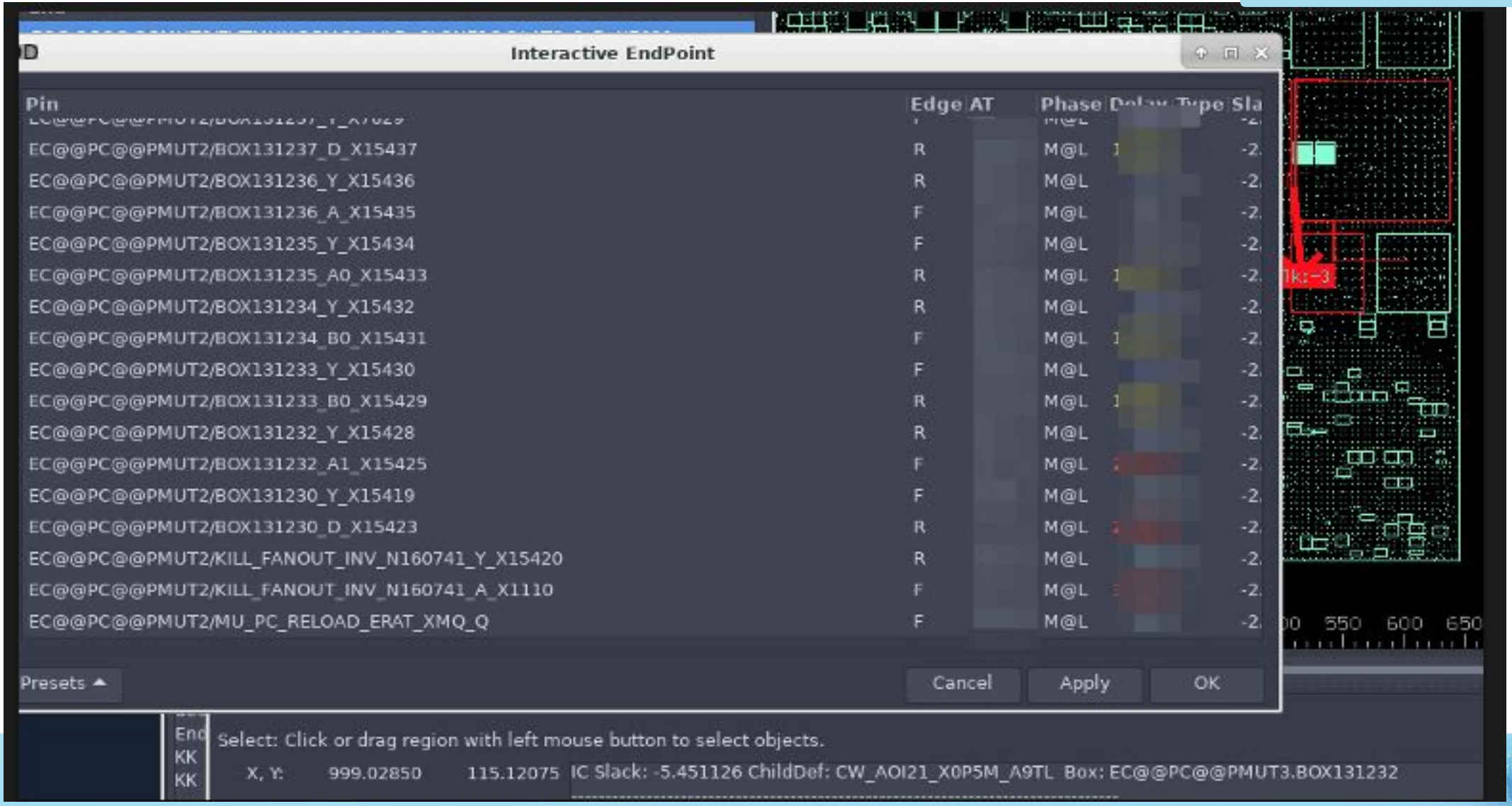
Challenge 1



- Utilizes Timing Visualizer database to locate and then **integrate all the pieces of hierarchy** back into a cohesive story
- Data is presented to our users in the format of an **interactive physical design browser** which enables exploration of both timing and physical information
- Can easily **navigate between levels of hierarchy**, as if all the design and analysis had been performed flat
- Secure REST APIs used to **securely communicate** between DDB and TimingVisualizer to obtain a variety of data including
  - Rules based timing triage recommendations
  - ML based timing triage recommendations
  - Manually assigned timing paths

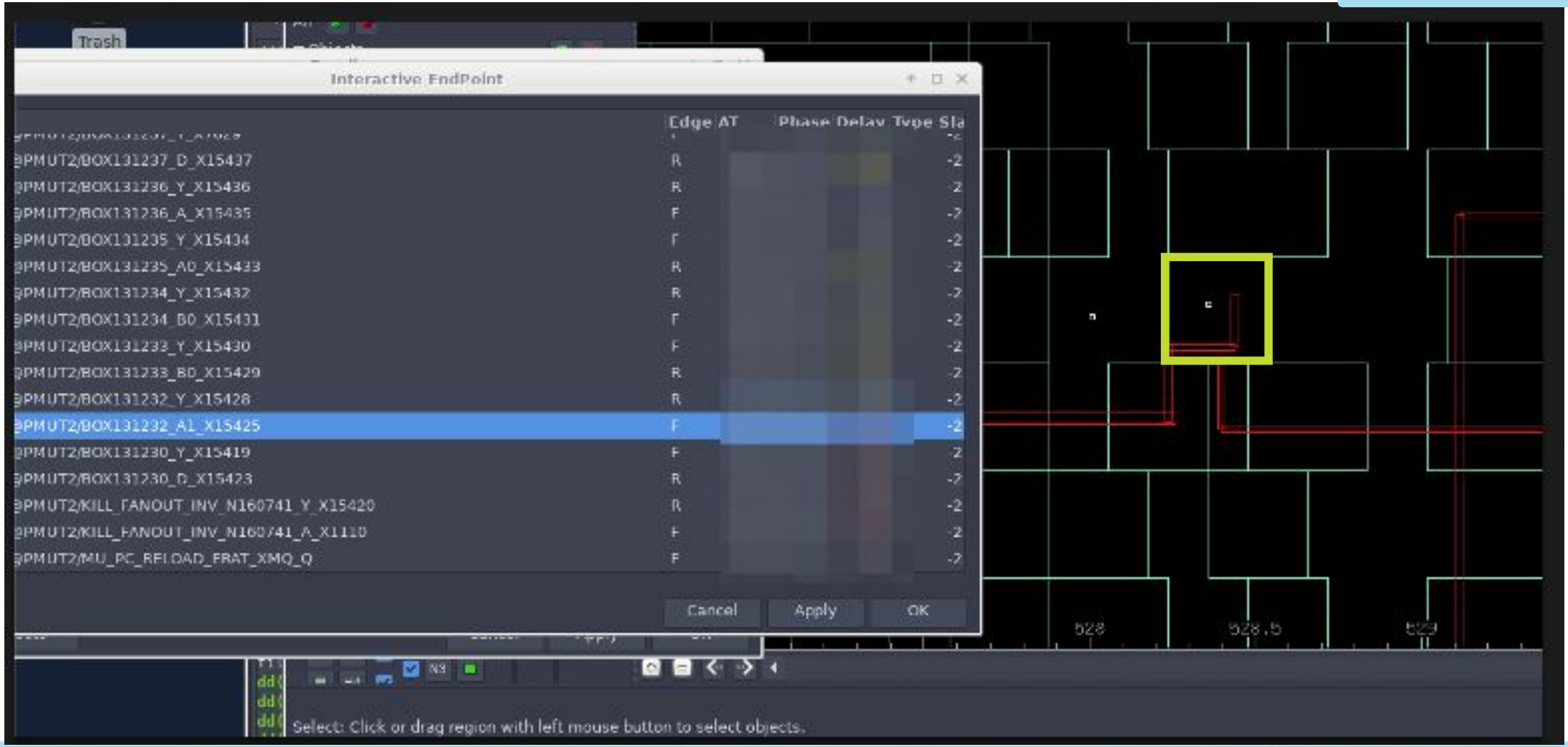
Interactively Generate End Point Report for Any Level of Hierarchy

Challenge 1

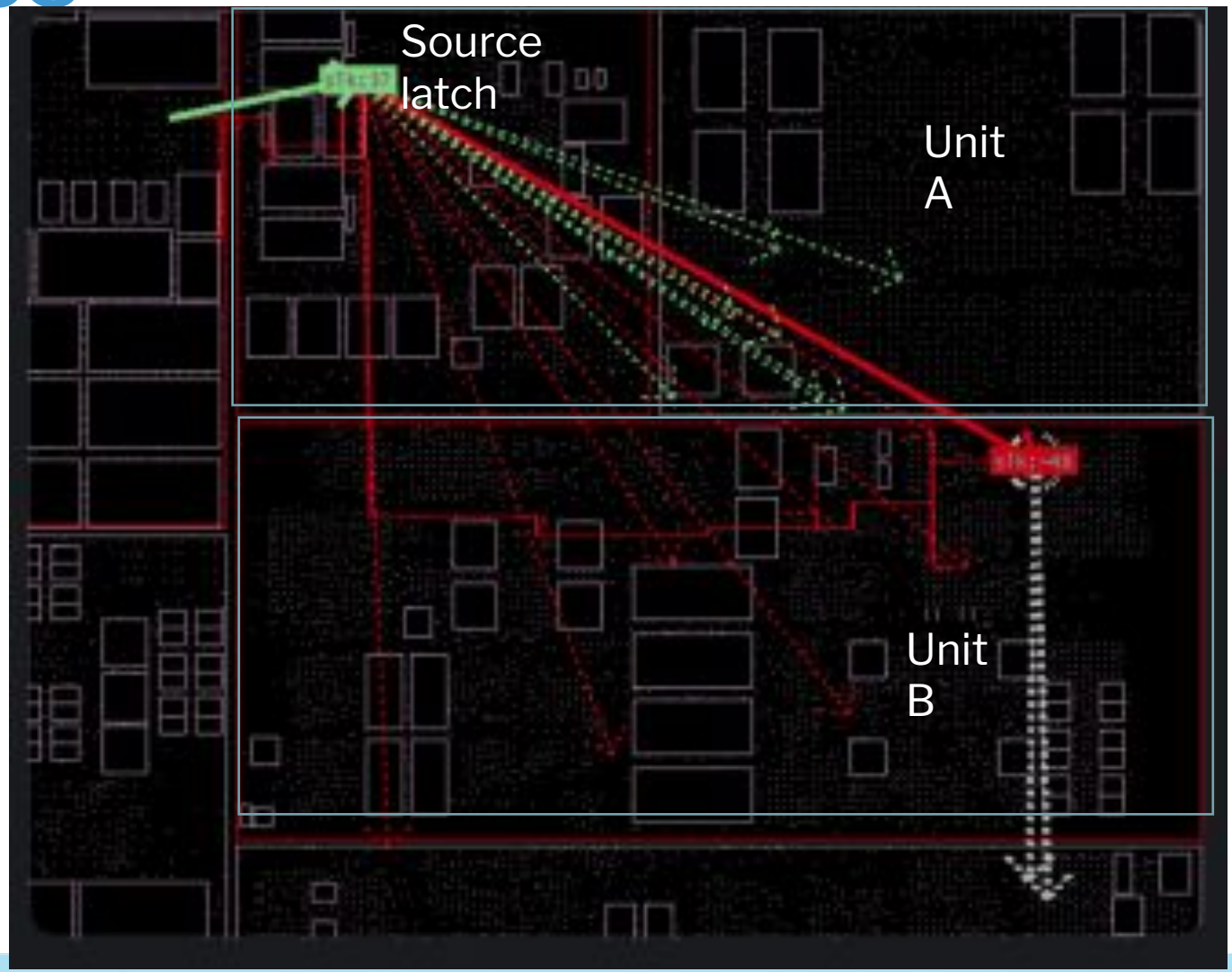


From Interactive Report, Zoom in to Any Circuit at Any Level of Hierarchy

Challenge 2



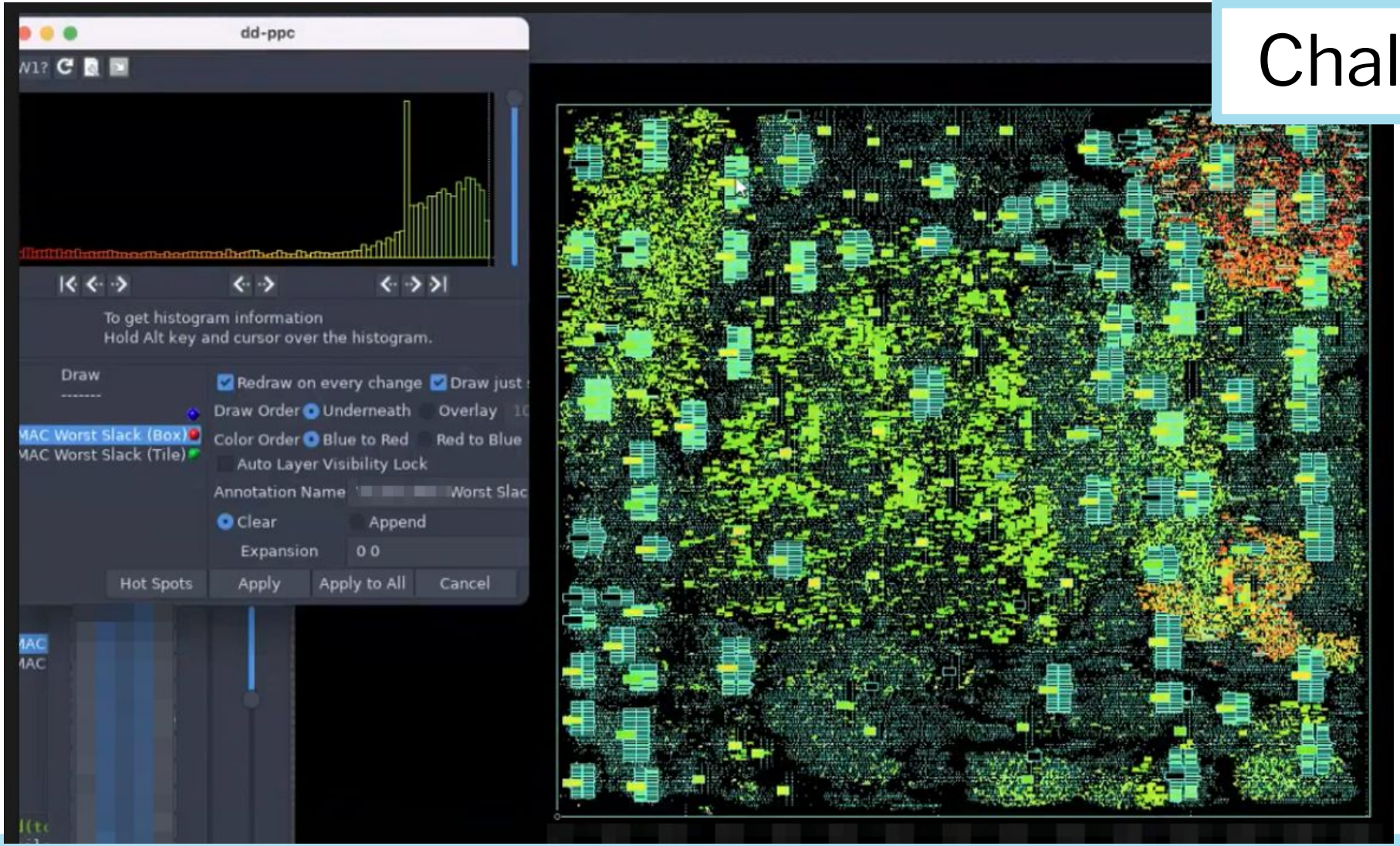
Explore Latch Fan-In/Out Across Multiple Cycles



Challenges 3 & 4

Interactively Generate Timing Heat-Maps

Challenge 2

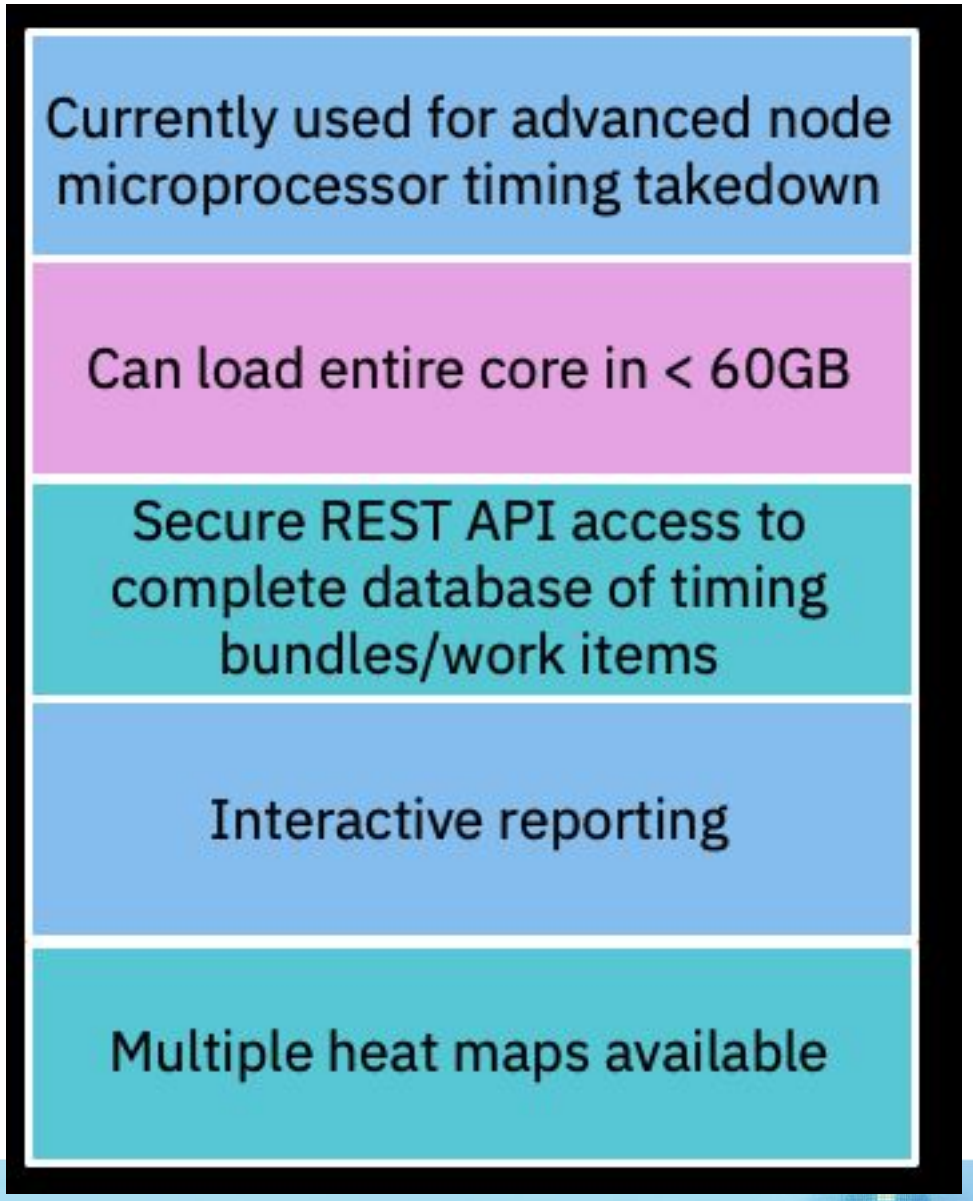


Summary

- Integration of timing visualizer web application with a high-performance X-windows based front end provides IBM microprocessor designers **unprecedented visualization and debug capabilities**.

- Timing analytics tools help answer hardware design questions **across hierarchy and time**, in both a high-level and low-level fashion.

- These tools help solve problems from initial proof-of-concept up to the completion of the design project.



JULY 9–13, 2023

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA